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EXAMINER	
SINGH, DALZID E	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,319	JIANG ET AL.	
	Examiner	Art Unit	
	Dalzid Singh	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,10,25,26,84-108 and 139* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10,25,26,84-108 and 139* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Transitional After Final Practice

1. The finality of the previous Office action is hereby withdrawn. Applicant's first submission after final filed on 21 February 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 84, 87-93, 96-98, 100-106 and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scharf et al (US Patent No. 6,369,924) in view of Gilliland et al (US Patent No. 6,160,647).

Regarding claim 84, Scharf et al disclose optical transceiver module, as shown in Figs. 1-6, comprising:

a housing for shielding the module (see col. 4, lines 18-21);

an optical block (25 shown in Fig. 6) having a first opening to receive a first optoelectronic device (the optoelectronic device (44 or 45) is shown in Fig. 6);

the first optoelectronic device (44 or 45) coupled into the first opening (see col. 5, lines 26-33);

a motherboard printed circuit board coupled to the housing (since the housing protects the mounting circuit board or motherboard, therefore, it would have been obvious that the housing is coupled to the motherboard; see col. 4, lines 18-21);

a first daughterboard printed circuit board (PCB) coupled to terminals of the first optoelectronic device in parallel to a first optical axis of the first optoelectronic device (26, 27 shown in Figs. 3 and 6 shows daughterboards coupled to the optoelectronic device (44 and 45)), the first daughterboard printed circuit board coupled at a first angle to the motherboard printed circuit board within the housing (as shown in Fig. 1, the daughterboard is coupled to the motherboard; see col. 5, lines 60-64; as shown in Fig. 6, the daughterboard is positioned in an angle).

Scharf et al disclose optical module as discussed above and differ from the claimed invention in that Scharf et al do not disclose that the optical module is coupled to a host system PCB. Gilliland et al is cited to show optical module comprising of connector pins (108) for coupling to host printed circuit board (PCB) (see col. 9, lines 43-48). Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made modify the optical system of Scharf et al by providing connector pins such as taught by Gilliland et al, in order to connect the optical module to a host PCB. One of ordinary skill in the art would have been motivated to do such in order to provide capability of communicating with other devices.

Regarding claim 87, as shown in Fig. 6, Scharf et al show that the first angle is substantially ninety degrees so that the first daughterboard printed circuit board is coupled perpendicular to the motherboard printed circuit board.

Regarding claims 88 and 98, the motherboard printed circuit board has a plurality of pins to couple to an external printed circuit board (since the motherboard or mounting board may be coupled to other devices, therefore the mother board has pins to coupled to such devices; see col. 4, lines 25-27).

Regarding claim 89, in Fig. 2, Scharf et al show the motherboard printed circuit board has a socket connector to couple to a socket connector of an external printed circuit board (see Fig. 2, Scharf et al show socket connector for connecting to external printed circuit board coupled to connector (24)).

Regarding claim 90, in Figs. 1-6, Scharf et al show the first daughterboard printed circuit board has traces coupled to traces of the motherboard printed circuit board.

Regarding claim 91, in col. 5, lines 57-64, Scharf et al disclose that the traces of first daughterboard printed circuit board are coupled traces of the motherboard printed circuit board by solder joints.

Regarding claim 101, in col. 5, lines 57-64, Scharf et al disclose that the traces of first daughterboard printed circuit board are coupled traces of the motherboard printed circuit board by solder joints, and the traces of second daughterboard printed circuit board are coupled traces of the motherboard printed-circuit board by solder joints.

Regarding claim 92, as shown in Fig. 6, Scharf et al show that the optical block further having a second opening to receive a second optoelectronic device (44 or 45), and wherein the fiber optic module further comprises, a second optoelectronic device coupled into the second opening, and a second daughterboard printed circuit board

(PCB) (26 or 27) coupled to terminals of the second optoelectronic device in parallel to a second optical axis of the second optoelectronic device, the second daughterboard printed circuit board coupled at a second angle to the motherboard printed circuit board.

Regarding claim 93, in col. 5, lines 26-33, Scharf et al disclose that the fiber optic module is a fiber optic transceiver and the first optoelectronic device is a transmitter (emitter) to couple photons into a first optical fiber, and the second optoelectronic device is a receiver to receive photons from a second optical fiber.

Regarding claim 96, as shown in Fig. 6, Scharf et al show that the first angle is substantially ninety degrees so that the first daughterboard printed circuit board is coupled perpendicular to the motherboard printed circuit board.

Regarding claim 97, as shown in Fig. 6, Scharf et al show that the second angle is substantially ninety degrees so that the second daughterboard printed circuit board is coupled perpendicular to the motherboard printed circuit board.

Regarding claim 100, in Figs. 1-6, Scharf et al show the first daughterboard printed circuit board has traces coupled to traces of the motherboard printed circuit board, and the second daughterboard printed circuit board has traces coupled to traces of the motherboard printed circuit board.

Regarding claim 102, in col. 4, lines 18-21, Scharf et al disclose housing having an opening at an end coupled to the motherboard printed circuit board.

Regarding claim 103, the first daughterboard printed circuit board and the second daughterboard printed circuit board each have a connector to couple to a connector of a host system printed circuit board through the opening at the end of the housing (since

the motherboard or mounting board may be coupled to other devices, therefore the mother board has pins to coupled to such devices; see col. 4, lines 25-27).

Regarding claim 104, shown in Fig. 1, the motherboard printed circuit board includes an inner septum to separate the fiber optic module into a first side and a second side (shown in Fig. 1 is the separation of pins on either side).

Regarding claim 105, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the inner septum is a conductive shield to reduce crosstalk and electromagnetic interference between the first and second daughterboards (as shown in Figs. 3 and 4, the EMI shield is provide between the first and second daughterboard, which reduces electromagnetic interference and therefore reduce crosstalk between the first and second daughterboards).

Regarding claim 106, in Fig. 6, Scharf et al show a housing includes an inner septum to separate the fiber optic module into a first side and a second side.

Regarding claim 108, as shown in Fig. 6, Scharf et al show the first and second daughterboard printed circuit boards are vertical printed circuit boards and the motherboard printed circuit board is a horizontal motherboard printed circuit board.

4. Claims 9, 10, 25, 26 and 139 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scharf et al (US Patent No. 6,369,924) in view of Gilliland et al (US Patent No. 6,160,647) and further in view of Mohr, III et al (US Patent No. 5,923,115).

Regarding claim 9, in Fig. 3 and in col. 5, lines 10-22 of Scharf et al, the combination discloses that the first daughterboard printed circuit board (26) further

comprises a ground plane (36a) on a backside thereof to reduce electro-magnetic interference (EMI) between the first and second optoelectronic devices (as shown in Fig. 3, the ground plane is provided on the daughterboards, therefore it would have been obvious to consider the ground plane as located on the backside of the first or second daughterboard). The combination differs from the claimed invention in that the combination does not disclose the ground plane reduce crosstalk. Mohr, III et al is cited to teach ground planes are provided to minimize crosstalk (see col. 10, lines 47-50). Therefore, since the combination provide ground plane (see Scharf et al), therefore the ground plane of the combination is able to reduce crosstalk.

Regarding claim 10, in Fig. 3 and in col. 5, lines 10-15 of Scharf et al, the combination discloses that the second daughterboard printed circuit board (27) further comprises a ground plane on a backside thereof to reduce electro-magnetic interference (EMI) between the first and second optoelectronic devices (as shown in Fig. 3, the ground plane is provided on the daughterboards, therefore it would have been obvious to consider the ground plane as located on the backside of the first or second daughterboard). The combination differs from the claimed invention in that the combination does not disclose the ground plane reduce crosstalk. Mohr, III et al is cited to teach ground planes are provided to minimize crosstalk (see col. 10, lines 47-50). Therefore, since the combination provide ground plane (see Scharf et al), therefore the ground plane of the combination is able to reduce crosstalk.

Regarding claim 25, in col. 5, lines 1-25 of Scharf et al, the combination discloses that the first daughterboard printed circuit board, shown in Fig. 3 and 4, further comprises:

first electrical components (42) coupled between the first optoelectronic device ((44) shown on Fig. 6) and the motherboard printed circuit board (see Fig. 1) on a front side of the first daughterboard in printed circuit board (26), the first electrical components for controlling the first optoelectronic device, and a first ground plane (36a) coupled to a back side of the first daughterboard internal printed circuit board to reduce electro-magnetic interference (EMI) between the first and second daughterboards; and,

wherein the second daughterboard in printed circuit board (27) further comprises: second electrical components (43) coupled between the second optoelectronic device ((45) shown on Fig. 6) and the motherboard printed circuit board (see Fig. 1) on a front side of the second internal printed circuit board, the second electrical components for controlling the second optoelectronic device (as shown in Fig. 3, the ground plane is provided on the daughterboards, therefore it would have been obvious to consider the ground plane as located on the backside of the first or second daughterboard). The combination differs from the claimed invention in that the combination does not disclose the ground plane reduce crosstalk. Mohr, III et al is cited to teach ground planes are provided to minimize crosstalk (see col. 10, lines 47-50). Therefore, since the combination provide ground plane (see Scharf et al), therefore the ground plane of the combination is able to reduce crosstalk.

Regarding claim 26, in col. 5, lines 1-25 of Scharf et al, the combination discloses that the second daughterboard printed circuit board ((27) shown in Fig. 3) further comprises: a second ground plane (37a) coupled to a back side of the second internal printed circuit board to reduce electro-magnetic fields (EMI) between the first and second daughterboard (as shown in Fig. 3, the ground plane is provided on the daughterboards, therefore it would have been obvious to consider the ground plane as located on the backside of the first or second daughterboard). The combination differs from the claimed invention in that the combination does not disclose the ground plane reduce crosstalk. Mohr, III et al is cited to teach ground planes are provided to minimize crosstalk (see col. 10, lines 47-50). Therefore, since the combination provide ground plane (see Scharf et al), therefore the ground plane of the combination is able to reduce crosstalk.

Regarding claim 139, , in col. 5, lines 10-15 of Scharf et al, the combination discloses wherein the first daughterboard printed circuit board further comprises a ground plane sandwiched between layers thereof to reduce electro-magnetic interference (EMI) between the first and second daughterboards (as shown in Fig. 3, the ground plane is provided on the daughterboards, therefore it would have been obvious to consider the ground plane as located on the backside of the first or second daughterboard). The combination differs from the claimed invention in that the combination does not disclose the ground plane reduce crosstalk. Mohr, III et al is cited to teach ground planes are provided to minimize crosstalk (see col. 10, lines 47-50). Therefore, since the combination provide ground plane (see Scharf et al), therefore the

ground plane of the combination is able to reduce crosstalk. Furthermore, it would have been obvious to provide the ground plane on the backside.

5. Claim 107 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scharf et al (US Patent No. 6,369,924) in view of Gilliland et al (US Patent No. 6,160,647) and further in view Mills et al (US Patent No. 5,647,748).

Regarding claim 107, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18 of Scharf et al, the combination discloses that the housing is a conductive shielded housing to encase the first daughterboard printed circuit board to reduce electromagnetic interference (EMI) and the septum ((35) shown in Fig. 3) is a conductive shield to reduce electromagnetic radiation (see col. 6, lines 13-18). The combination differs from the claimed invention in that the combination does not disclose the EMI shield reduces crosstalk. Mills is cited to teach that EMI is associated with crosstalk (see col. 2, lines 8-11). Therefore, since the conductive septum of the combination shield against EMI, therefore it would have been obvious that the conductive septum also reduce crosstalk.

6. Claims 85 and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scharf et al (US Patent No. 6,369,924) in view of Gilliland et al (US Patent No. 6,160,647) and further in view of Grosser et al (US Patent No. 6,118,667).

Regarding claim 85, in col. 4, lines 18-21 of Scharf et al, the combination discloses housing coupled to the motherboard printed circuit board coupled with connector pins (see Fig. 1). The combination differs from the claimed invention in that the combination does not provide tabs extending from the housing coupled to slots in the motherboard. Grosser et al teach the use of pins or tab for coupling to motherboard (see col. 3, lines 54-59). Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide coupling to the motherboard through the use of pins or tabs.

Regarding claim 86, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the housing is a shielded housing to encase the first daughterboard printed circuit board to reduce electromagnetic interference (EMI).

7. Claims 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scharf et al (US Patent No. 6,369,924) in view of Gilliland et al (US Patent No. 6,160,647) and further in view of Poplawski et al (US Patent No. 6,267,606).

Regarding claim 94, in col. 4, lines 18-21, Scharf et al disclose a housing coupled to the motherboard printed circuit board and differ from the claimed invention in that Scharf et al do not disclose clips on the housing coupled to clip openings on the motherboard. Poplawski et al is cited to show clip from the housing coupled to motherboard (see col. 20, lines 67 to col. 21, lines 1-2). Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide clips so that the housing could be coupled to the motherboard. One of ordinary

skill in the art would have been motivated to do such in order to secure the housing to the motherboard.

Regarding claim 95, in col. 4, lines 38 to 54, col. 5, lines 5-25 and col. 6, lines 13-18, Scharf et al disclose that the housing is a shielded housing to encase the first daughterboard printed circuit board to reduce electromagnetic interference.

8. Claim 99 is rejected under 35 U.S.C. 103(a) as being unpatentable over Scharf et al (US Patent No. 6,369,924) in view of Gilliland et al (US Patent No. 6,160,647) and further in view of Dell et al (US Patent No. 6,108,730).

Regarding claim 99, the combination of Scharf et and Gilliland et al differs from the claimed invention in the combination does not disclose the motherboard printed circuit board has a socket connector to couple to a socket connector of an external printed circuit board. Dell et al is cited to show motherboard has a socket connector to couple to a socket connector of a printed circuit board (see col. 5, lines 35-37). Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to provide socket to the motherboard in order to enable communication with other communication devices.

Response to Arguments

9. Applicant's arguments with respect to claims 9, 10, 25, 26, 84-108 and 139 have been considered but are moot in view of the new ground(s) of rejection.

10. Applicant's arguments filed 21 February 2006 have been fully considered but they are not persuasive.

Applicant argues that Scharf et al do not comprise a motherboard. In col. 4, lines 16-17, Scharf et al disclose motherboard or mounting circuit board. Applicant further indicates that the invention is for mounting on a host PCB. The secondary reference to Gilliland et al is provided to teach transceiver coupled to PCB (col. 9, lines 43-48 of Gilliland et al).

Applicant further argues that the ground planes of Scharf et al are on the front side of the PCB. Scharf et al disclose ground planes on the circuit boards along with EMI shield to reduce or prevent EMI (see col. 5, lines 10-25). Scharf et al do not disclose the ground planes are on the front or backside. However, since either side of the circuit board can be considered as front or back, therefore, it would have been obvious to indicate the ground plane as located on the backside.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalzid Singh whose telephone number is (571) 272-3029. The examiner can normally be reached on Mon-Fri 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DS
March 23, 2006

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